10/039651 C of C

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October 31, 2005

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: **CERTIFICATE OF CORRECTION**
U. S. Letters Patent No. 6,931,505 B2
Issued: August 16, 2005
For: DISTRIBUTED MEMORY MODULE CACHE COMMAND FORMATTING
Inventor: David
Our File No. 42390.P13872

Dear Sir:

Enclosed is the Certificate of Correction (two copies) for the above-referenced patent.

This request for correction is made under rule 322 of the Rules of Practice and 35 U.S.C. Section 254.

Also enclosed is a copy of the amended claims dated March 7, 2005, and the Notice of Allowance accepting those claims. Please note that the response to the communication of 09/07/2005 as indicated by the Notice of Allowance is a print error on the part of the PTO. No correspondence was made on the date indicated. Thus, we wish to clarify the communication date as being March 7, 2005.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Edwin H. Taylor
Reg. No. 25,129

EHT/jsq
Enclosures

DEC 13 2005

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. :6,931,505 B2

DATED : August 16, 2005

INVENTOR(S) : David

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 9, at line 7, delete "tage" and insert --tag--.

In column 9, lines 10-11, delete ", the command sequencer and serializer unit to control the data cache located on the memory module".

In column 9, at line 12 after "lines,", insert --each of--.

In column 9, at line 13 before "sequentially", insert --including a plurality of segments--.

In column 9, at the end of line 14, delete "command" and insert --segment--.

In column 9, at line 15 after "periods,", insert --wherein--.

In column 9, at line 16, delete "including" and insert --include--.

In column 9, at line the end of line 16 after "command", insert to read data from a memory device of the memory module--.

In column 9, at line 17 after "cache fetch command", insert --to fetch data from the data cache of the memory module--.

In column 9, at line 20 after "transfer periods", insert --, while a remainder of the segments of the activate command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical--.

In column 9, at line 59 after "memory bus", delete --, the memory controller component including an array of tag address storage locations--.

In column 9, at line 61 before "the commands", insert --each of--.

In column 9, at line 61 after "the commands", insert --including a plurality of segments--.

In column 9, at line 63 after "transaction", insert --and each of the segments being delivered within one of the transfer periods--.

In column 9, at line 63 before "the plurality", insert --wherein--.

In column 9, at line 63 after "of commands", delete "including" and insert --include--.

In column 9, at line 63 after "activate command", insert --to read data from the at least one memory device--.

In column 9, at line 64 after the second occurrence of "command", insert --to fetch data from the data cache--.

MAILING ADDRESS OF SENDER
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
12400 Wilshire Blvd. 7th floor
Los Angeles, CA 90025-1026

PATENT NO. 6,931,505

Certificate of Correction (PTO Form 1050)-Amended

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PATENT NO. : 6,931,505 B2

DATED : August 16, 2005

INVENTOR(S) : David

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 9, at line 68, after "periods", insert --,while a remainder of the segments of the activate command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical.--.

In column 10, at line 27, after "controller," , insert --each of--.

In column 10, at line 27, after "commands", insert --including a plurality of segments--.

In column 10, at line 29, after "transaction", insert --and each of the segments being delivered within one of the transfer periods, wherein--.

In column 10, at line 30, delete "including" and insert --include--.

In column 10, at line 30, after "command", insert --to read data from the at least one memory device--.

In column 10, at line 31, after "command," insert --to fetch data from the data cache--.

In column 10, at line 34, after "periods", insert --,while a remainder of the segments of the activate command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical.--..

In column 10, at line 64, after "command," , insert --while a remainder of the segments of the activate command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical.--.

In column 12, at line 5, after "command" ,insert --,while a remainder of the segments of the read command and the read and preload command transferred during transfer periods other than the last transfer period remains substantially identical.--.

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In column 9, at line 61 before "the commands", insert --each of--.

In column 9, at line 61 after "the commands", insert --including a plurality of segments--.

In column 9, at line 63 after "transaction", insert --and each of the segments being delivered within one of the transfer periods--.

In column 9, at line 63 before "the plurality", insert --wherein--.

In column 9, at line 63 after "of commands", delete "including" and insert --include--.

In column 9, at line 63 after "activate command", insert --to read data from the at least one memory device--.

In column 9, at line 64 after the second occurrence of "command", insert --to fetch data from the data cache--.

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In column 10, at line 27, after "commands", insert --including a plurality of segments--.

In column 10, at line 29, after "transaction", insert --and each of the segments being delivered within one of the transfer periods, wherein--.

In column 10, at line 30, delete "including" and insert --include--.

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In column 10, at line 31, after "command," insert --to fetch data from the data cache--.

In column 10, at line 34, after "periods", insert --,while a remainder of the segments of the activate command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical.---..

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PATENT NO. 6,931,505

Certificate of Correction (PTO Form 1050)-Amended

DEC 1 3 2005

Notice of Allowability

Application No.	Applicant(s)	
10/039,651	DAVID, HOWARD S.	
Examiner	**Art Unit**	
Zhuo H Li	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *0907/2005*.

2. ☒ The allowed claim(s) is/are *1-28*.

3. ☒ The drawings filed on *31 December 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

MATTHEW D. ANDERSON
PRIMARY EXAMINER

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
LOS ANGELES

Application No.: 10/039,651 **Filing/Issue Date:** 12/31/2001 **Docket No.:** 042390.P13872
Date Mailed: 03/01/2005 **Due Date(s):** 03/03/2005
Client: Intel Corporation **Atty/Sec:** EHT/MGM/KGS/dmc
Title: Distributed Memory Module Cache Command Formatting
First Named Inventor: Howard S. David

The following has been received in the U.S.P.T.O. on the date stamped hereon:

Transmittal Letters & Certificate of Mailing
- ☒ Transmittal Letter
- ☒ Fee Transmittal (original & copy)
- ☐ RCE (Request for Continued Examination)
- ☐ Transmittal of Formal Drawings
- ☐ Issue Fee Transmittal (original & copy)
- ☐ Certificate of
- ☐ Express Mail No.:

Missing Parts, Formal Papers
- ☐ Response to Notice of Missing Parts
- ☐ Assignment & Cover sheet (_____ pgs.)
- ☐ Declaration & POA (_____ pgs.)

Amendment / Response
- ☒ Amendment/Response Response (15 pgs.)
- ☐ Terminal Disclaimer
- ☐ Other:

Petitions & Appeals
- ☐ Petition for Extension of Time:
- ☐ Notice of Appeal
- ☐ Appeal Brief & two copies (_____ pgs. each)
- ☐ Reply Brief (_____ pgs.)

Other
- ☐ Information Disclosure Statement & PTO/SB/08 (_____ pgs.) (previously 1449)
- ☐ Request to Publish (Rescind NonPublication)
- ☐ Drawings: _____sheets, _____figures
- ☒ Postcard

Checks
- ☐ Check No. _____ Amount $_____
- ☐ Check No. _____ Amount $_____

IN THE CLAIMS

Please amend claims 1, 13, 19, 25, and 27 as indicated below.

1. (Currently Amended) A memory controller, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations to receive information regarding whether there is a cache hit from the array of [[tage]] tag address storage locations, the command sequencer and serializer unit to control a data cache located on a memory module using the received information~~, the command sequencer and serializer unit to control the data cache located on the memory module~~ by delivering a plurality of commands over a plurality of command and address lines, each of the commands including a plurality of segments sequentially delivered over a plurality of transfer periods of a memory access transaction and each segment ~~command~~ being delivered within one of the transfer periods,

wherein the plurality of commands ~~including~~ include an activate command to read data from a memory device of the memory module and a cache fetch command to fetch data from the data cache of the memory module, the activate and cache fetch commands differing in format only in the information delivered during a last transfer period of the plurality of transfer periods, while a remainder of the segments of the activate command and the cache fetch command transferred

during transfer periods other than the last transfer period remains substantially identical.

2. (Previously Presented) The memory controller of claim 1, the activate command and the cache fetch command differing in cache hit information delivered during the last transfer period.

3. (Previously Presented) The memory controller of claim 2, the cache fetch command further including way information delivered during the last transfer period.

4. (Previously Presented) The memory controller of claim 3, the plurality of commands each delivered over four transfer periods.

5. (Previously Presented) The memory controller of claim 4, the activate and cache fetch commands each including memory module destination information during a first transfer period.

6. (Previously Presented) The memory controller of claim 5, the activate and cache fetch commands each including row address information during each of the four transfer periods.

7. (Previously Presented) The memory controller of claim 1, the plurality of commands further including a read command and a read and preload command, the read and read and preload commands differing in format only in the information delivered during a last transfer period.

8. (Previously Presented) The memory controller of claim 7, the read command and read and preload command differing in cache hit information delivered during the last transfer period.

9. (Previously Presented) The memory controller of claim 8, the read and preload command further including way information delivered during the last transfer period.

10. (Previously Presented) The memory controller of claim 9, the plurality of commands each delivered over four transfer periods.

11. (Previously Presented) The memory controller of claim 10, the read command and the read and preload command each including memory module destination information during a first transfer period.

12. (Previously Presented) The memory controller of claim 11, the read command and read and preload command each including column address information during each of the four transfer periods.

13. (Currently Amended) A memory module, comprising:

at least one memory device; and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller component over a plurality of command lines of a memory bus~~, the memory controller component including an array of tag address storage locations~~, each of the commands including a plurality of segments sequentially delivered over a plurality of transfer periods of a memory access transaction and each of the segments being delivered within one of the transfer periods,

wherein the plurality of commands ~~including~~ include an activate command to read data from the at least one memory device and a cache fetch command to fetch data from the data cache, the activate and cache fetch commands differing in format only in the information delivered during a last transfer period of the plurality transfer periods, while a remainder of the segments of the activate command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical.

14. (Previously Presented) The memory module of claim 13, the activate command and the cache fetch command differing in cache hit information delivered during the last transfer period.

15. (Previously Presented) The memory module of claim 14, the cache fetch command further including way information delivered during the last transfer period.

16. (Previously Presented) The memory module of claim 15, the plurality of commands each delivered over four transfer periods.

17. (Previously Presented) The memory module of claim 16, the activate and cache fetch commands each including memory module destination information during a first transfer period.

18. (Previously Presented) The memory module of claim 17, the activate and cache fetch commands each including row address information during each of the four transfer periods.

19. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

a memory module coupled to the memory controller via a memory bus, the memory module including

at least one memory device, and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, each of the commands including a plurality of segments sequentially delivered over a plurality of transfer periods of a memory access transaction and each of the segments being delivered within one of the transfer periods,

wherein the plurality of commands ~~including~~ include an activate command to read data from the at least one memory device and a cache fetch command to fetch data from the data cache, the activate and cache fetch commands differing in format only in the information delivered during a last transfer period of the plurality of transfer periods, while a remainder of the segments of the activate command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical.

20. (Original) The system of claim 19, the activate command and the cache fetch command differing in cache hit information delivered during the last transfer period.

21. (Original) The system of claim 20, the cache fetch command further including way information delivered during the last transfer period.

22. (Original) The system of claim 21, the plurality of commands each delivered over four transfer periods.

23. (Original) The system of claim 22, the activate and cache fetch commands each including memory module destination information during a first transfer period.

24. (Original) The system of claim 23, the activate and cache fetch commands each including row address information during each of the four transfer periods.

25. (Currently Amended) A method, comprising:

sequentially delivering during a plurality of transfer periods of a memory access transaction information corresponding to both an activate command and a cache fetch command from a memory controller to a memory module over a plurality of command lines of a memory bus, the information being partitioned into a plurality of segments corresponding to the plurality of transfer periods and each segment being transmitted via one of the commands lines within one of the plurality of transfer periods; and

delivering from the memory controller to the memory module during a last transfer period of the plurality of transfer period associated with the memory access transaction information differentiating between an activate command and a cache fetch command, while a remainder of the segments of the activate

command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical.

26. (Previously Presented) The method of claim 25, wherein delivering during a last transfer period information differentiating between an activate command and a cache fetch command includes delivering one of cache way and cache hit information.

27. (Currently Amended) A method, comprising:

sequentially delivering during a plurality of transfer periods information corresponding to both a read command and a read and preload command from a memory controller to a memory module over a plurality of command lines of a memory bus, the information being partitioned into a plurality of segments corresponding to the plurality of transfer periods and each segment being transmitted via one of the commands lines within one of the plurality of transfer periods; and

delivering from the memory controller to the memory module during a last transfer period of the plurality of transfer period associated with the memory access transaction information differentiating between a read command and a read and preload command, while a remainder of the segments of the read command and the read and preload command transferred during transfer periods other than the last transfer period remains substantially identical.

28. (Previously Presented) The method of claim 27, wherein delivering during a last transfer period information differentiating between a read command and a read and preload command includes delivering one of cache way, eviction buffer, and cache hit information.

IN THE SPECIFICATION

Please amend paragraph [0016] of page 5 as follows:

[0016] In this example embodiment, the memory controller 202 is coupled to the memory modules 220, 230, 240, and 250 via a point-to-point interconnect 265. The interconnect 265 may include [[8]] 18 differential pairs, 9 pairs for data, and 9 pairs for address and command. The interconnect may transfer data at a rate several times the rate of the buffer to DRAM interconnect. Another embodiment may use 27 differential pairs, 18 pairs for data, and 9 pairs for address and command. The interconnect 265 may also include 18 differential pairs, 9 pairs for read data, and 9 pairs for write data, address and command. Still other embodiments are possible using a wide range of interconnect techniques and numbers of signals.